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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Hisanori FUJISAWA

Serial No.: 09/045,041 Group Art Unit: 2123

Confirmation No.: 9340 Examiner: H. Jones

Filed: March 20, 1998 Appeal No.:

For: METHOD AND APPARATUS FOR CARRYING OUT CIRCUIT SIMULATION

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REPLY BRIEF

Responsive to the Examiner's Answer mailed August 12, 2003 and pursuant to 37 C.F.R. 1.193(b)(1), the following comments are provided in reply.

Status of Claims

In section (3) on page 2 of the Examiner's Answer, the Examiner stated that the status of the claims contained in the Appellant's Appeal Brief is incorrect. However, the Status of Claims in the Appeal Brief reflects the status of the claims according to the final Office Action mailed November 27, 2002.

Summary of Invention

The Summary

In section (5) on page 3 of the Examiner's Answer, the Examiner disagreed with Appellant's Summary of Invention in the Appeal Brief filed May 22, 2003 as not having "mapped the claims" to the Summary of Invention. Appellant submits that the requirements of MPEP §

1200 have been satisfied. Nonetheless, for additional clarity, the features of claim 9 are read on the specification and drawings, as follows.

Claim 9 recites a method of carrying out simulation of a circuit. In the method of claim 9, data are input (Fig. 4 at 4 and page 15, lines 21-33 of the specification) that include configurations (page 19, lines 22-23 of the specification) for a plurality of partial circuits (e.g., partial circuits 11 and 12 of Fig. 9), and connectional relationships (page 14, lines 24-26 of the specification) for input and output terminals of the partial circuits.

Next, the plurality of partial circuits to inspect for equivalent operational characteristics are extracted from the circuit to be simulated (Fig. 5 at S11 and page 14, lines 16-21 and page 19, lines 15-19 of the specification). Then, the plurality of partial circuits are inspected (page 12, line 31 through page 13, line 4 of the specification) to detect partial circuits exhibiting equivalent operational characteristics (Fig. 5 at S13 and page 19, lines 21-33 and page 24, lines 2-11 of the specification), based on the configurations (Fig. 5 at S12) of the plurality of partial circuits, and equivalence is judged (Fig. 5 at S16 and Figs. 9 and 11; and page 20, lines 8-12, page 23, line 26 through page 24, line 11, and page 24, line 36 through page 25, line 10 of the specification) when the configurations of the plurality of partial circuits are mutually consistent (Fig. 5 at S12).

Finally, the circuit is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit (Fig. 13 and page 26, lines 27-37 of the specification) and simulating the compressed circuit (Fig. 3 at S4 and page 13, lines 4-8 and page 27, lines 1-15 of the specification).

The Background

In section (5) on page 4 of the Examiner's Answer, the Examiner objected to the Summary of Invention in the Appeal Brief at page 4, second full paragraph, to page 5, first full paragraph, as being "argumentative in nature." However, this portion of the Summary of Invention was provided merely as background for the invention and was intended to provide a greater understanding of the invention.

The Quasi-Equivalence Feature

In section (5) on page 4 of the Examiner's Answer, the Examiner stated that "most" of the Summary of Invention was directed to the "quasi-equivalence" feature recited in dependent claims 19, 31, and 43. However, only three of the 13 paragraphs of the Summary of Invention discuss the quasi-equivalence feature. Appellant notes that the quasi-equivalence feature was described in the Summary of Invention to provide greater understanding of this feature, which was recited in claims that had been rejected in the final Office Action mailed November 27, 2002.

Grouping of Claims

In section (7) on page 4 of the Examiner's Answer, the Examiner stated that the "appellant's statement in the brief that certain claims **do not** stand or fall together is not agreed with because Appellant's brief does not include a statement that this grouping of claims **does not** stand or fall together and reasons in support thereof" (emphasis added). However, the claims "stand or fall together," as recited in the Grouping of claims section on page 6 of the Appeal Brief.

In section (7) on page 4 of the Examiner's Answer, the Examiner stated that Appellant has not "actually argued any" of the claims on pages 8-13 of the Appeal Brief and has only referred to the prior art without referring to any of the claims. However, independent claims 9, 21, and 33 are recited on page 7 under the Argument section of the Appeal Brief and claim language was specified in the arguments on pages 8-13. For example, the second paragraph on page 10 of the Appeal Brief states that "it is submitted that the hierarchical test generation technique of Chakrabarti does not teach or suggest the circuit simulation of the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit," which contains language recited in independent claims 9, 21, and 33. Because the claims stand or fall together, it is submitted that the requirements of 37 C.F.R. 1.192(c)(7) and MPEP § 1200 have been satisfied.

Arguments

In section (11) on pages 7-9 of the Examiner's Answer, the Examiner has introduced additional reasons for rejecting the claims. The Examiner has asserted on pages 7 and 8 of the Examiner's Answer that the first sentence of the abstract of Chakrabarti discloses all features of claim 9, for example. The first sentence of the abstract of Chakrabarti recites the following: "An improved hierarchical testing algorithm for combinational circuits with repetitive sub-circuits using the bus fault model. This model exploits the regularity of a circuit by grouping together identical gate-level sub-circuits into high-level sub-circuits."

The Examiner also asserted on pages 8 and 9 of the Examiner's Answer that "grouping together identical gate-level sub-circuits into high-level sub-circuits based upon the characteristics of logical operations" is equivalent to the feature of the present invention of integrating a plurality of partial circuits that are determined to exhibit equivalent operational characteristics into one partial circuit, as recited in claim 9, for example. The Examiner further asserted that "logical operations" in a logic device refers to operational behavior.

Chakrabarti discloses a hierarchical test generation technique for combinational circuits with repetitive sub-circuits, in which gate-level sub-circuits are determined to exhibit equivalent characteristics based on the characteristics of logical operations. For illustrative purposes, six circuits are shown in the attached Appendix 1 and Appendix 2. Because the circuits of Example 1 and Example 2 have equivalent logical operations, Chakrabarti would determine that the circuits of Example 1 and Example 2 exhibit equivalent characteristics and would group these circuits together as identical gate-level sub-circuits. However, because the circuits of Example 1 and Example 3 do not have equivalent logical operations, Chakrabarti would not determine that the circuits of Example 1 and Example 3 exhibit equivalent characteristics and would not consider these circuits to be identical gate-level sub-circuits.

In contrast, in the present invention, a plurality of partial circuits are determined to exhibit equivalent operational characteristics based upon the **physical** configurations and operational characteristics of the partial circuits. For example, unlike Chakrabarti, the present invention would not determine that the circuits shown in Example 1 and Example 2 are equivalent because the type of logic gate (NAND gate) connected to input terminals C and D in the circuit of Example 1 differs from the type of logic gate (NOT gate) connected to input terminals C and D in the circuit of Example 2. Thus, in the present invention, the circuits of Example 1 and

Example 2, viewed from input terminals C and D, are not considered as being equivalent to one another.

Further, unlike Chakrabarti, because the type of logic gate (NAND gate) connected to input terminals C and D in the circuit of Example 1 is the same as the type of logic gate (NAND gate) connected to input terminals C and D in the circuit of Example 3, the present invention would consider the two NAND gates in these circuits as being identical partial circuits. These NAND gates would then be integrated into one circuit in the present invention.

Thus, in Chakrabarti, two sub-circuits merely need to exhibit equivalent logical operations to be grouped together as identical gate-level sub-circuits. Internal circuit configurations are not inspected for equivalence. In contrast, in the present invention, **internal** circuit configurations are inspected to detect partial circuits exhibiting equivalent operational characteristics. When two partial circuits exhibiting equivalent operational characteristics are detected, the two partial circuits are integrated into one circuit in the present invention.

For example, Chakrabarti would determine that the circuit of Example 4 and the circuit of Example 5 have equivalent logical operations. However, Chakrabarti would not then inspect the internal circuit configurations of Example 4 and Example 5.

In contrast, in the present invention, the internal circuit configurations of Example 4 and Example 5 would be inspected for equivalence. Specifically, considering Example 6, the present invention would analyze the internal circuit configurations of logic circuits S1 and S2 to detect partial circuits exhibiting equivalent operational characteristics. When two partial circuits exhibiting equivalent operational characteristics are detected in logic gates S1 and S2, respectively, these two partial circuits are integrated into one circuit.

Conclusion

In summary, it is submitted that Chakrabarti does not teach or suggest inspecting a plurality of extracted partial circuits to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of the plurality of partial circuits, determining equivalence when the configurations of the plurality of partial circuits are mutually consistent, and compressing the circuit to be simulated by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and simulating the compressed circuit.

Thus, Appellant submits that claims 9-12, 14-24, 26-36, and 38-44 patentably distinguish over the prior art. Accordingly, Appellant respectfully requests reversal of the Examiner's rejections.

The Commissioner is authorized to charge any unpaid fees required for the filing of this Reply Brief to Deposit Account No. 19-3935.

Respectfully submitted,
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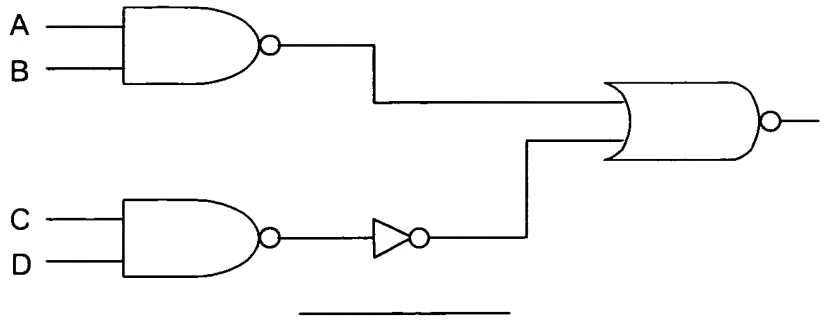
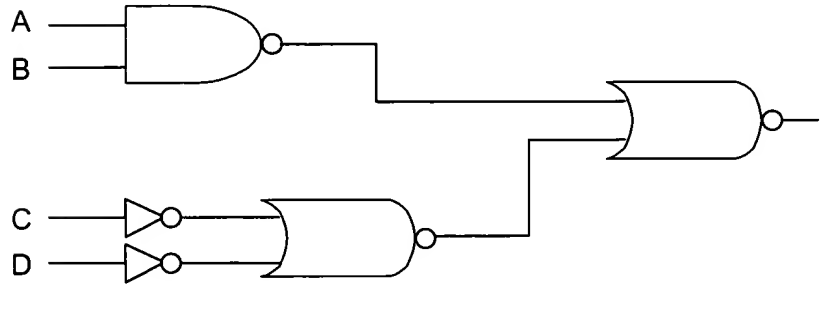
APPENDIX 1

Example 1



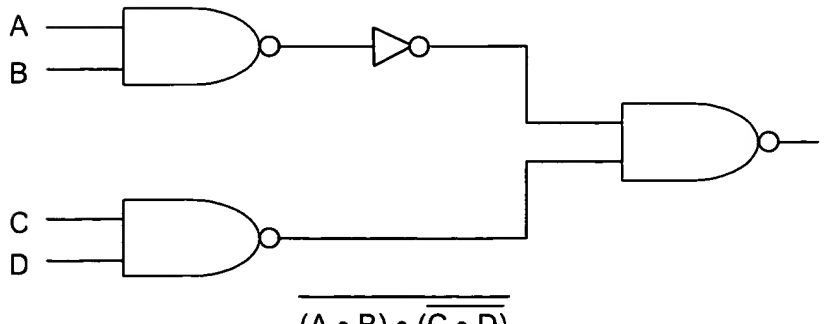
$\overline{\overline{(A \bullet B)} + (C \bullet D)}$

Example 2



$\overline{\overline{(A \bullet B)} + (C \bullet D)}$

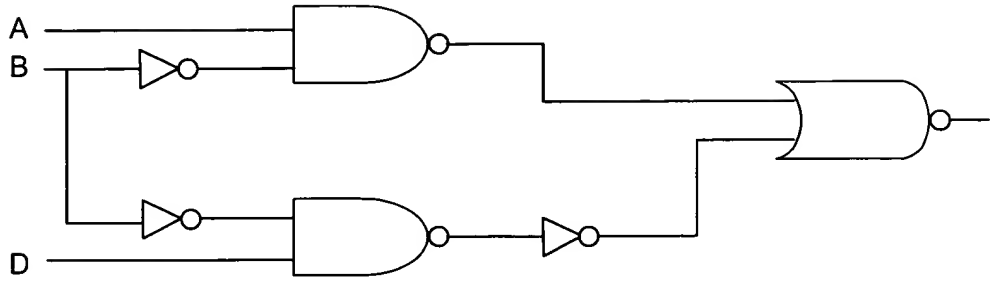
Example 3



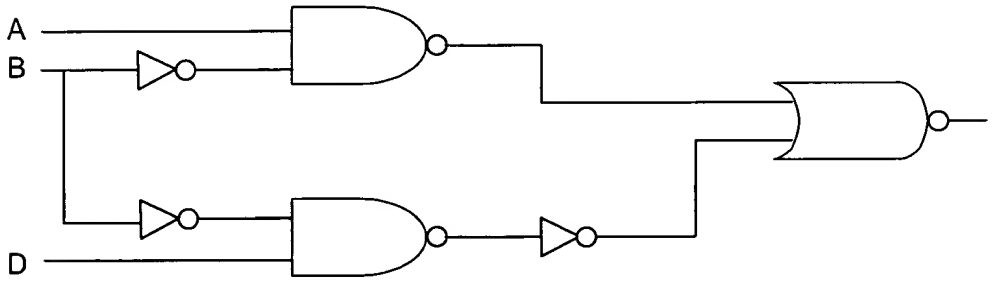
$\overline{(A \bullet B) \bullet \overline{(C \bullet D)}}$

APPENDIX 2

Example 4



Example 5



Example 6